

## MIMO 4x4 QR Decomposition IP Core

### Key Features

- Supports a variety of matrix dimensions, up to 4X4
- Computes the upper triangular matrix R and rotations corresponding to the unitary matrix Q
- Efficient implementation and low gate count
- Up to 20M 4X4 matrices per second
- Easily synthesizable for various ASIC and FPGA implementations

### Functional Description

QR decomposition is one of the most useful matrix decompositions. Specifically, any  $N \times M$  (complex) matrix  $\mathbf{H}$  may be decomposed into a product of two matrices

$$\mathbf{H} = \mathbf{Q}\mathbf{R}$$

where  $\mathbf{R}_{N \times M}$  is an upper triangular matrix with real diagonal, and  $\mathbf{Q}_{N \times N}$  is a unitary matrix, satisfying  $\mathbf{Q}^* \mathbf{Q} = \mathbf{I}$ .

The QR decomposition is a powerful tool in numerous applications. For example, the standard solution of a linear system

$$\mathbf{x}_{N \times 1} = \mathbf{H}_{N \times N}^{-1} \mathbf{y}_{N \times 1}$$

requires the highly complex inversion of an  $N \times N$  matrix. Using the QR decomposition of  $\mathbf{H}$ , the solution simplifies to

$$\mathbf{x} = (\mathbf{Q}\mathbf{R})^{-1} \mathbf{y} = \mathbf{R}^{-1} \mathbf{Q}^* \mathbf{y} \Rightarrow \mathbf{R}\mathbf{x} = \mathbf{Q}^* \mathbf{y}$$

which is easily solved by back-substitution since  $\mathbf{R}$  is upper triangular.

The core is fed with the matrix  $\mathbf{H}_{N \times M}$  where  $N \geq M$ , and computes  $\mathbf{R}$  and a set of rotations representing  $\mathbf{Q}$ .

A functional block diagram of this core is given in Fig. 1.

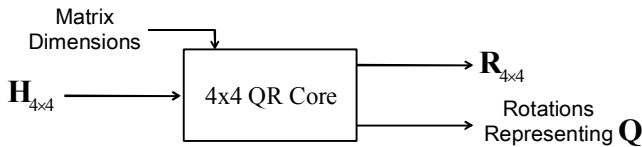


Figure 1: Functional Block Diagram

### Resources

Synthesis results on several FPGA devices are listed in Table 1.

Device	A	B
Clock Frequency (MHz)	155	159
Slice Registers	8286 (1%)	50642 (8%)
Slice LUT	8181 (2%)	21961 (7%)
On-Chip Memory Blocks	0	0
Dedicated Multipliers	36 (2%)	36 (4%)

A: Xilinx Virtex<sup>®</sup>-7 XCV7585t

B: Altera Stratix<sup>®</sup>-V 5SGXEA5N2F45C2

Table 1: Characteristics of the QR core on selected FPGA Devices

### Greenair Wireless

2 Koifmann St.  
 Tel Aviv  
 Israel

Tel: + 972 (3)5161030  
 Fax: + 972 153543108451

Email: [contact@greenairwireless.com](mailto:contact@greenairwireless.com)  
 web: [www.greenairwireless.com](http://www.greenairwireless.com)

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### Core Performance

In order to assess the performance of the QR IP Core, we incorporated the core into a linear MIMO detector. Simulations comparing fixed-point and floating-point implementations were carried out in uncorrelated Rayleigh fading channels. The results for 64QAM with rate 5/6 are given in Fig. 2. As shown the gaps between floating-point and fixed-point are below 0.2dB for all MIMO modes.

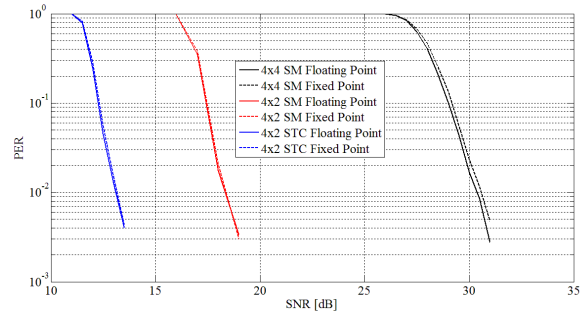


Figure 2: Performance of fixed-point implementation and comparison with floating point

### Applications

QR Decompositions play a fundamental role in ubiquitous MIMO applications (LTE, LTE-A, IEEE802.11, IEEE802.16). These include:

- OFDM/OFDMA per tone MIMO decoding
- SC-FDMA MIMO decoding
- Sphere decoding
- SIC/PIC MIMO decoding
- MIMO link adaptation and LTE RS demodulation

### Deliverables

- Fully-commented and synthesizable VHDL source code or FPGA netlist
- Bit exact C software model
- Product manual and detailed documentation
- Technical support

### Related Products

- 4x4 Least Squares
- 4x4 Near-Optimal MIMO Maximum Likelihood (ML) Detector

### Ordering Information

For purchasing or to obtain more detailed information on this product or any of our other products or services, please contact Greenair Wireless. We will be pleased to discuss how we can address your special requirements.